DCR750F85

Phase Control Thyristor

DS5934-3 July 2014 (LN31717)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- Medium Voltage Soft Starts
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR750F85* DCR750F80 DCR750F75 DCR750F70	8500 8000 7500 7000	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 200mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.
*8200V @ -40^0 C, 8500V @ 0^0 C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

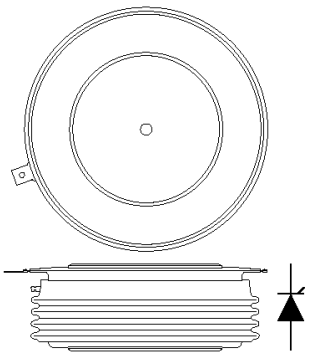
DCR750F85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	8500V
$I_{T(AV)}$	733A
I_{TSM}	9800A
dV/dt*	1500V/µs
dI/dt	200A/µs

* **Higher dV/dt selections available**



Outline type code: F

(See Package Details for further information)

Fig. 1 Package outline

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	733	A
$I_{T(RMS)}$	RMS value	-	1151	A
I_T	Continuous (direct) on-state current	-	1139	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	9.8	kA
I^2t	I^2t for fusing	V_R = 0	0.48	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0184	°C/W
		Single side cooled	Anode DC	-	0.0333	°C/W
			Cathode DC	-	0.0418	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 23 kN (with mounting compound)	Double side	-	0.004	°C/W
			Single side	-	0.008	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			20.0	25.0	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	200	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	100	A/µs
		Gate source 30V, 10Ω, t_r < 0.5µs, T_j = 125°C	Non-repetitive	-	200	A/µs
$V_{T(TO)}$	Threshold voltage – Low level	100A to 500A at T_{case} = 125°C		-	1.030	V
	Threshold voltage – High level	500A to 2500A at T_{case} = 125°C		-	1.30	V
r_T	On-state slope resistance – Low level	100A to 500A at T_{case} = 125°C		-	2.06	mΩ
	On-state slope resistance – High level	500A to 2500A at T_{case} = 125°C		-	1.542	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω, t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	T_j = 125°C, I_{peak} = 1000A, t_p = 1000us, V_R = 100V, dI/dt = 5A/µs, dV_{DR}/dt = 20V/µs linear to 2500V		-	1200	µs
I_{RR}	Reverse Recovery current	I_T = 1000A, tp = 1000us, T_j = 125°C, dI/dt = – 5A/µs, V_{Rpeak} = 100V		95	118	A
Q_S	Stored charge			3000	4000	µC
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V_{DRM}, T_{case} = 125°C	0.4	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	350	mA
I_{GD}	Gate non-trigger current	At 50% V_{DRM}, T_{case} = 125°C	10	mA

CURVES

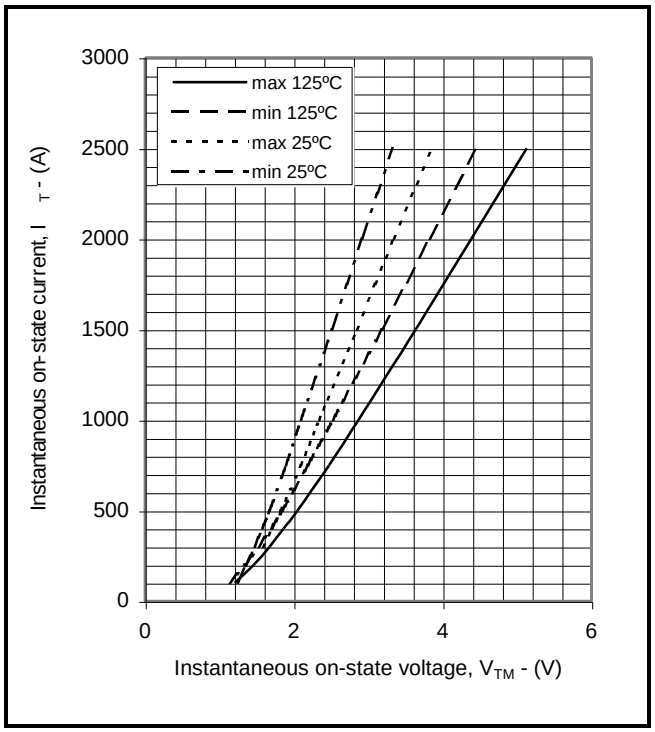


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$V_{TM} = A + B\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.454245
B = 0.106933
C = 0.001271
D = 0.013218

these values are valid for T_j = 125°C for I_T 100A to 3000A

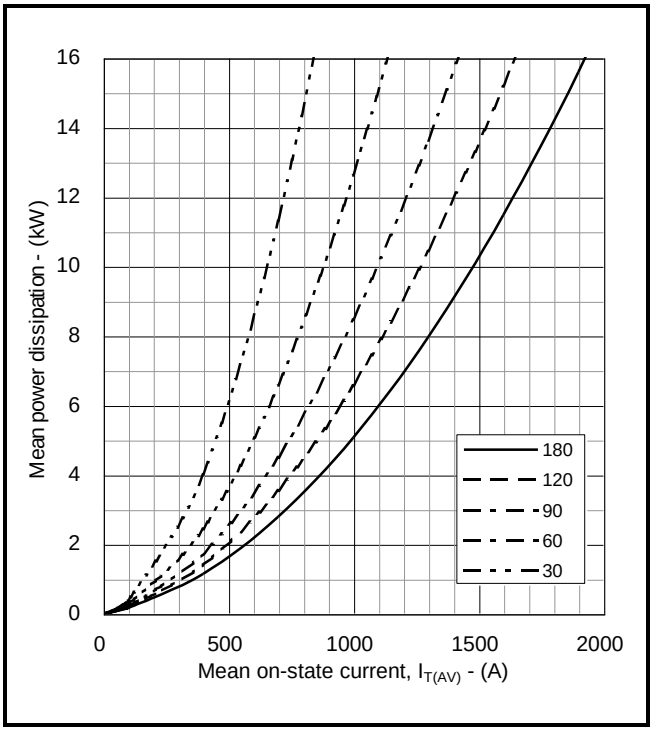


Fig.3 On-state power dissipation – sine wave

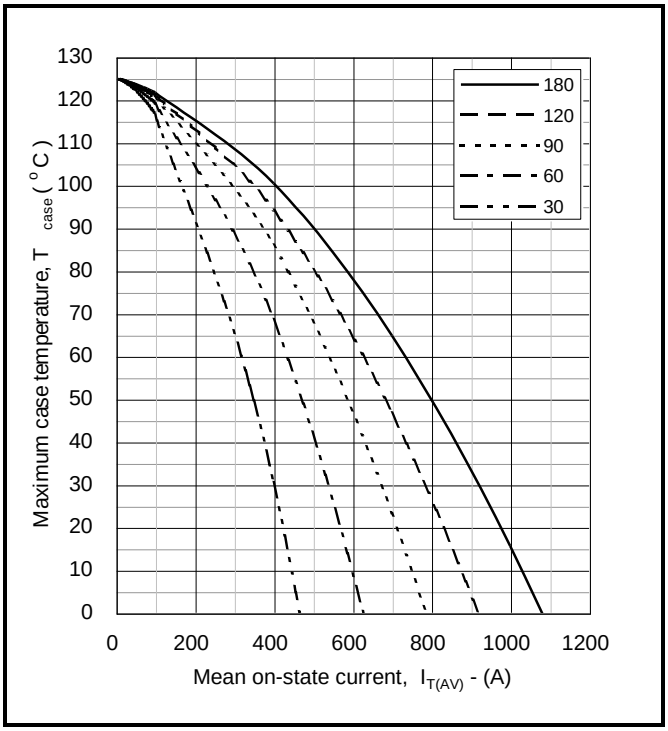


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

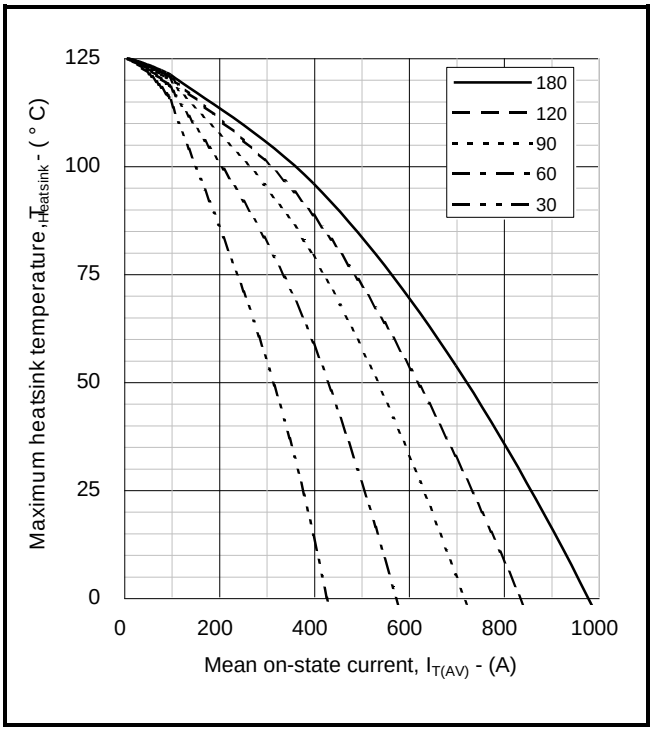


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

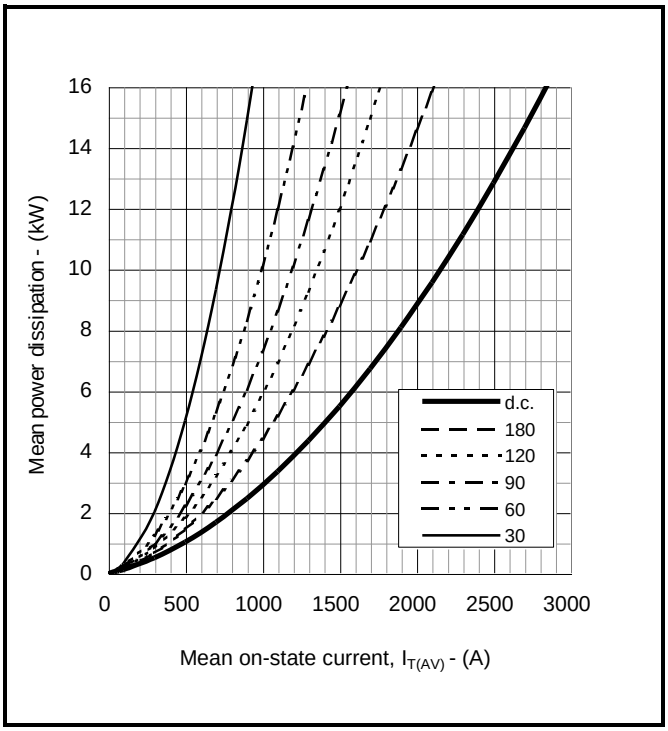


Fig.6 On-state power dissipation – rectangular wave

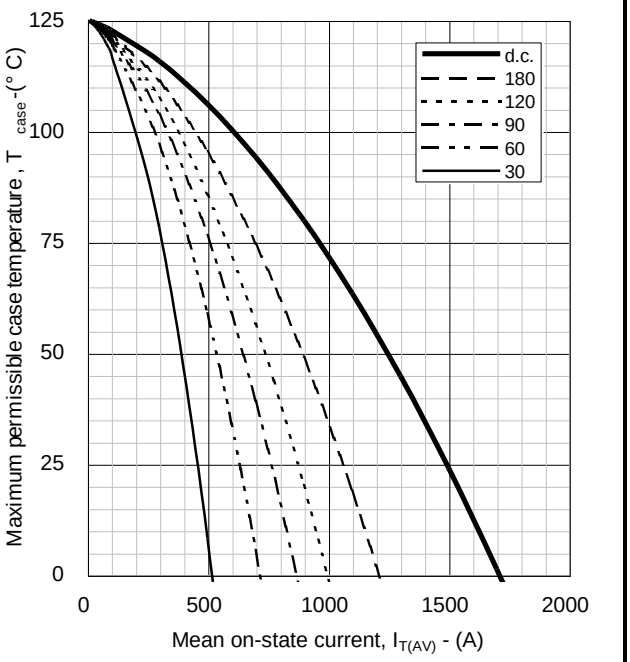


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

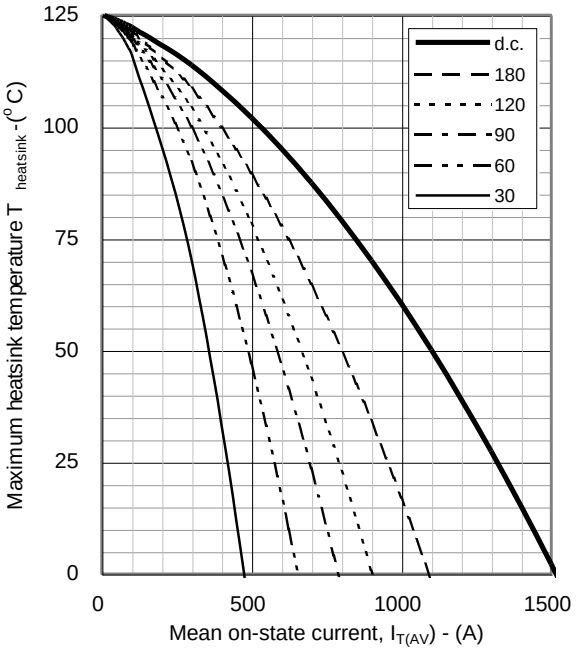
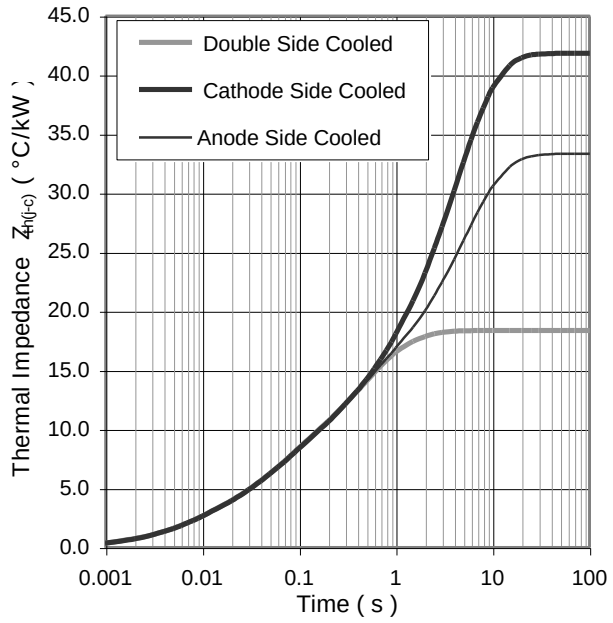


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R_i (°C/kW)	7.5608	4.0772	3.8420	2.8671
	T_i (s)	0.6877	0.2537	0.0614	0.0101
Anode side cooled	R_i (°C/kW)	6.7211	4.6219	15.5387	14.8631
	T_i (s)	0.1910	0.0158	5.0011	3.3169
Cathode side cooled	R_i (°C/kW)	11.5564	8.5810	4.7942	8.3643
	T_i (s)	4.2216	6.0269	0.0166	0.2255

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(-T/T_i))]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	3.19	2.14
120	3.72	3.10
90	4.29	3.64
60	4.81	4.23
30	5.22	4.88
15	5.40	5.22

Anode Side Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	2.97	2.03
120	3.43	2.89
90	3.92	3.36
60	4.36	3.87
30	4.69	4.41
15	4.84	4.70

Cathode Sided Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	2.95	2.02
120	3.40	2.87
90	3.88	3.34
60	4.31	3.84
30	4.64	4.37
15	4.79	4.65

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

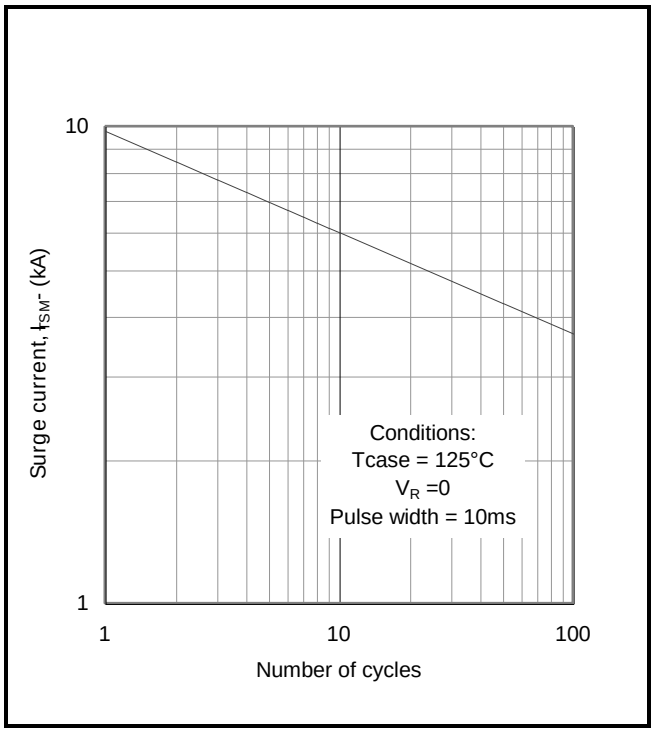


Fig.10 Multi-cycle surge current

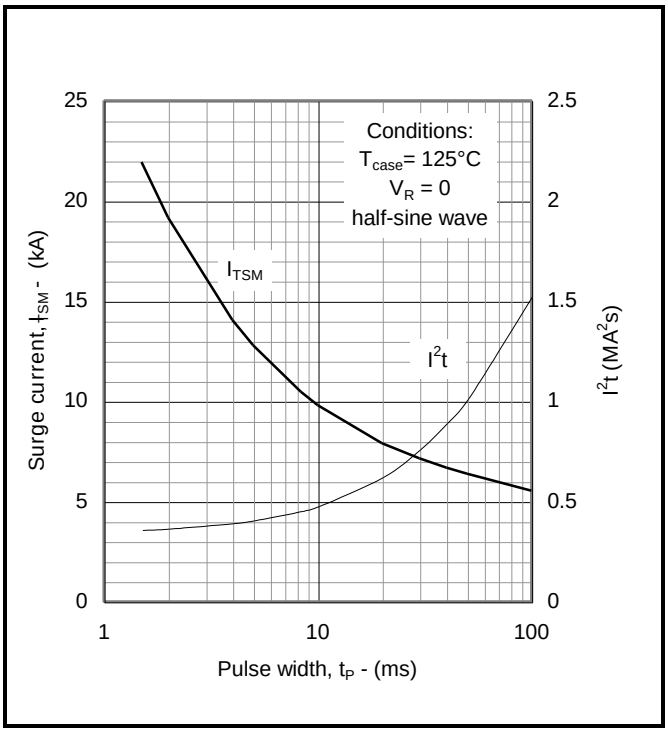


Fig.11 Single-cycle surge current

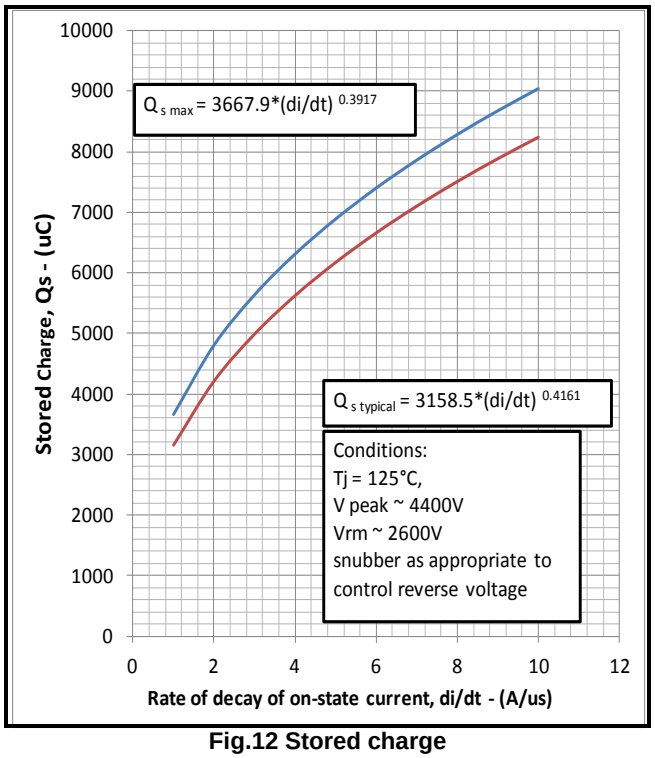


Fig.12 Stored charge

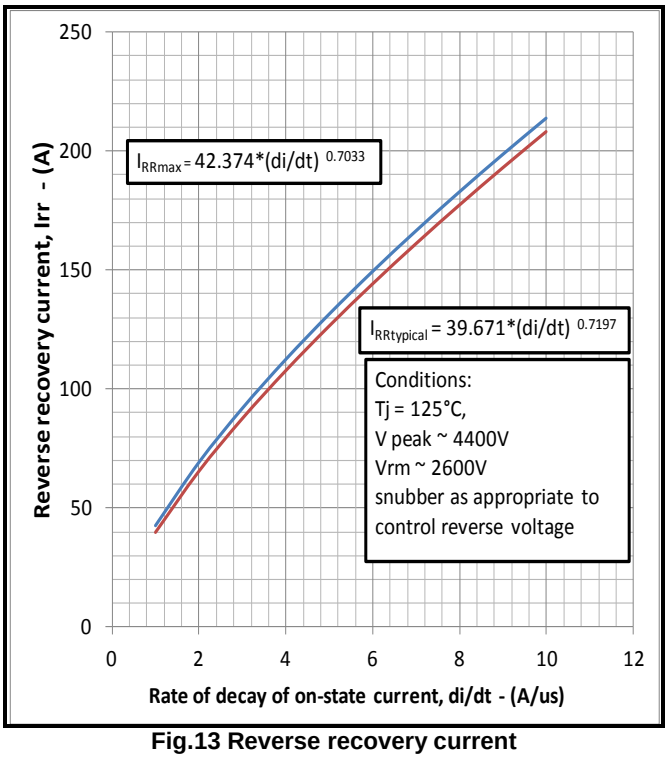


Fig.13 Reverse recovery current

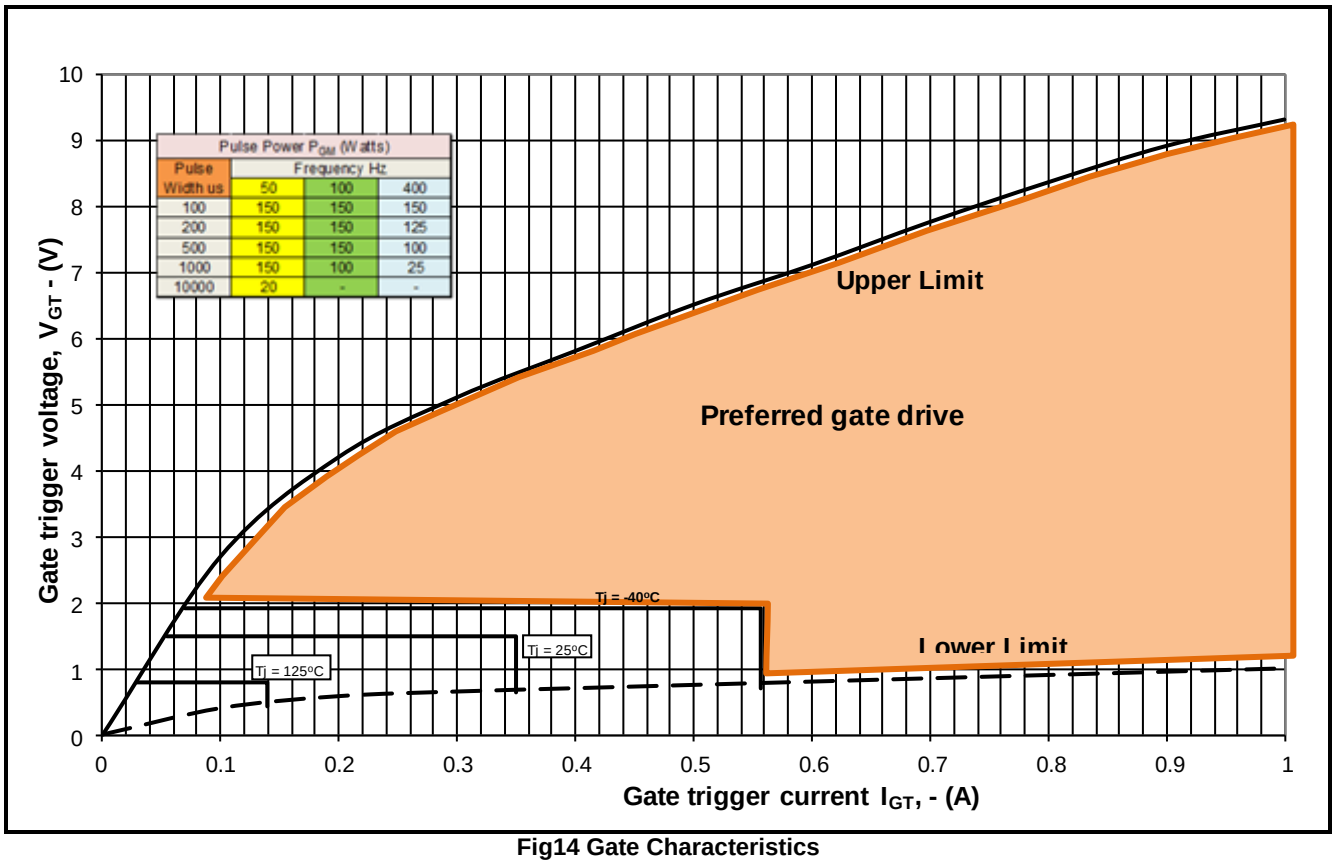


Fig14 Gate Characteristics

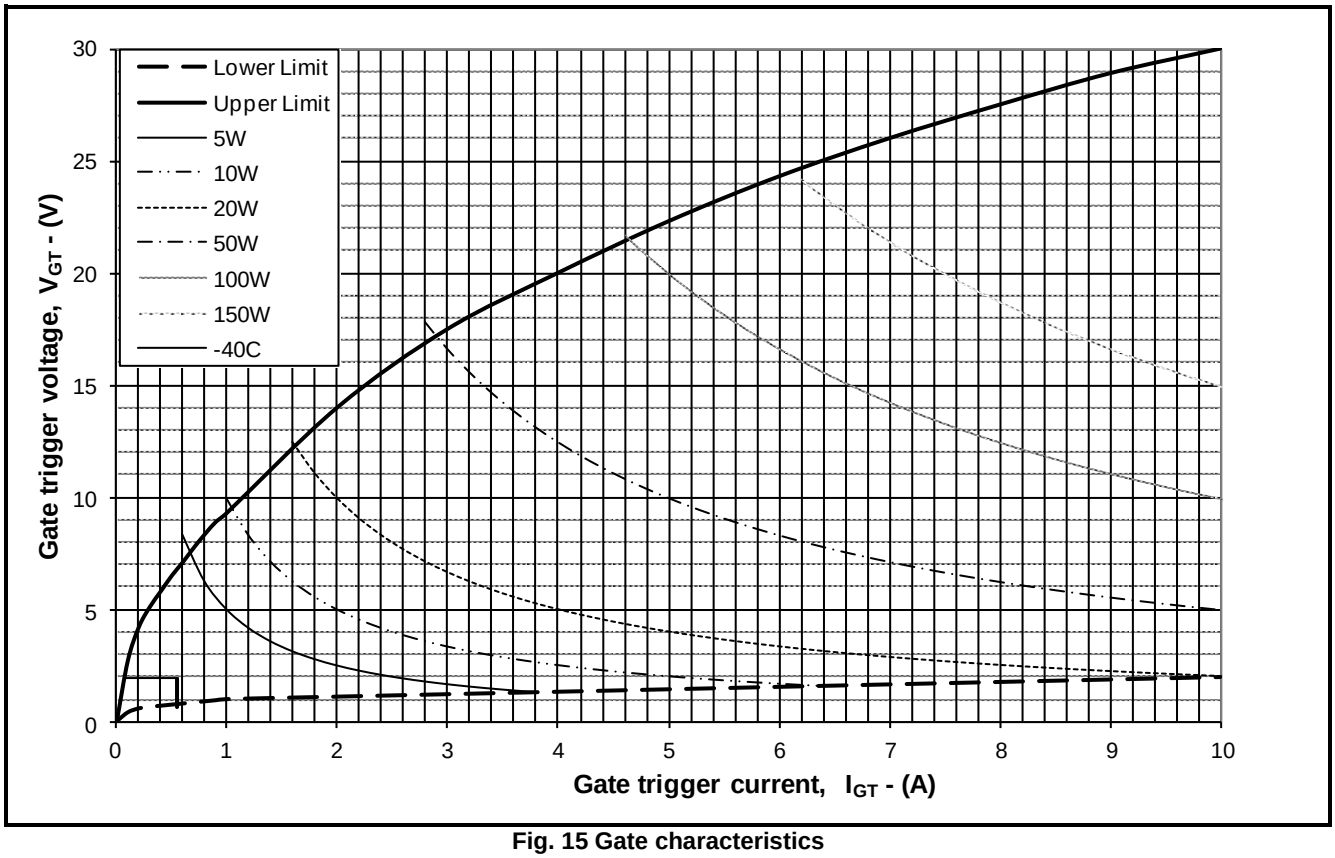


Fig. 15 Gate characteristics

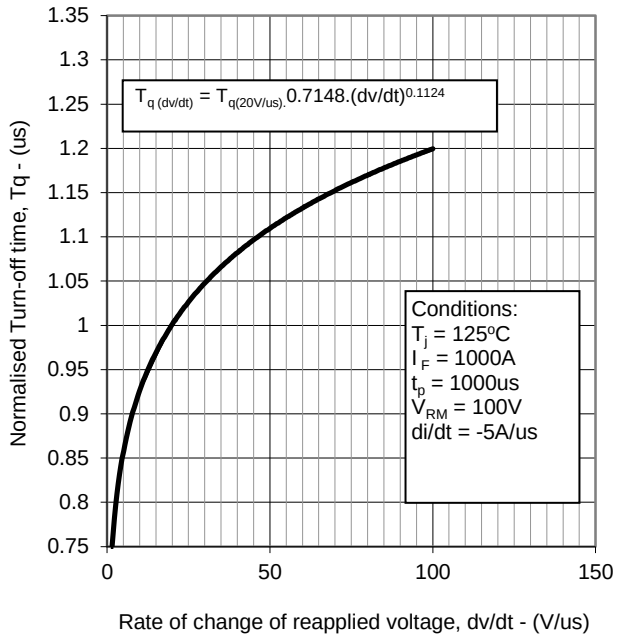
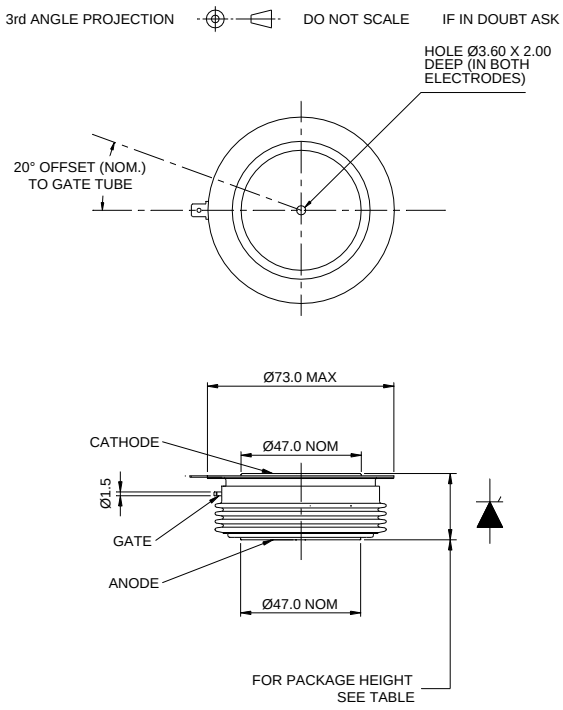


Fig.16 Turn-off time

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR1003SF18	26.415	25.865
DCR1006SF28	26.49	25.94
DCR1008SF36	26.72	26.17
DCR1020F65	27.1	26.55
DCR1050SF42	26.72	26.17
DCR1180F52	26.84	26.29
DCR1274SF18	26.415	25.865
DCR1275SF28	26.49	25.94
DCR1277SF36	26.72	26.17
DCR1279SF48	26.84	26.29
DCR1350F42	26.72	26.17
DCR1610F28	26.49	25.94
DCR1640F28	26.49	25.94
DCR1830F22	26.415	25.865
DCR750F85	**27.46**	**26.91**
DCR810F85	27.46	26.91
DCR840F48	26.84	26.29
DCR890F65	27.1	26.5
DCR950F65	27.1	26.5

Lead length: 420mm
Lead terminal connector: M4 ring

Package outline type code: F

Fig.17 Package outline

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Extended exposure to conditions outside the product ratings may affect reliability leading to premature product failure. Use outside the product ratings is likely to cause permanent damage to the product. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture, a large current to flow or high voltage arcing, resulting in fire or explosion. Appropriate application design and safety precautions should always be followed to protect persons and property.

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